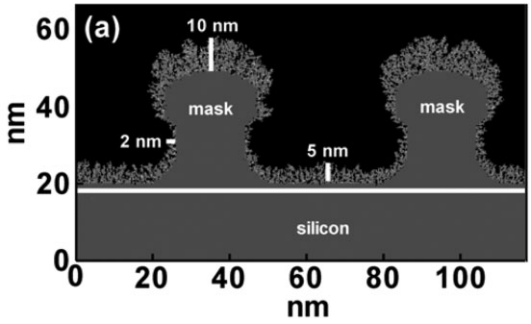
Formation of a Nanoscale SiO_2 Capping Layer on Photoresist Lines with an $Ar/SiCl_4/O_2$ Inductively Coupled Plasma: A Modeling Investigation

Stefan Tinck,* Efrain Altamirano-Sánchez, Peter De Schepper, Annemie Bogaerts

PECVD of a nanoscale SiO_2 capping layer using low pressure $SiCl_4/O_2/Ar$ plasmas is numerically investigated. The purpose of this capping layer is to restore photoresist profiles with improved line edge roughness. A 2D plasma and Monte Carlo feature profile model are applied for this purpose. The deposited films are calculated for various operating conditions to obtain a layer with desired shape. An increase in pressure results in more isotropic deposition with a higher deposition rate, while a higher power creates a more anisotropic process. Dilution of the gas mixture with Ar does not result in an identical capping layer shape with a thickness linearly correlated to the dilution. Finally, a substrate bias seems to allow proper control of the vertical deposition rate versus sidewall deposition as desired.



1. Introduction

Integrated circuits have consistently been manufactured with smaller feature sizes over the years, allowing more components to be packed on each chip.[1] The increased functionality per given area reduces the cost per chip. However, fulfilling this continuous decrease in electronic feature size in the 21st century is not obvious. Indeed, putting more transistors on an integrated circuit inevitably means creating smaller component structures. Since the dimensions of parts of the components are currently reaching the nanoscale range, the downscaling of reliable electronic devices becomes increasingly more difficult and eventually limited. Over the last forty years, the technology node dropped from 10 μm in 1971 to 20 nm in 2013.[2] This technology node can be considered as the smallest half-pitch of contacted metal lines where the pitch is the size of a repeating unit on the wafer. In the case of shallow trench isolation (STI), it is equal to the sum of the width of a photoresist line and the width of the trench between the photoresist lines. STI can be considered as the first step in chip manufacturing, even before transistors are fabricated. Indeed, to isolate active

S. Tinck, A. Bogaerts
Research Group PLASMANT, Department of Chemistry, University of Antwerp, Universiteitsplein 1, B-2610, Antwerp, Belgium
E-mail: stefan.tinck@ua.ac.be
E. Altamirano-Sánchez, P. De Schepper
IMEC, Kapeldreef 75, B-3001 Leuven, Belgium

Plasma Process. Polym. **2014,** *11*, 52–62

DOI: 10.1002/ppap.201300062

areas on the wafer surface, shallow trenches are etched in the Si wafer, and subsequently filled with isolating material such as SiO_2. Basically, this process starts with creating photoresist lines (mask patterning) to define where the silicon will be selectively etched. As feature dimensions decrease, the pitch between photoresist lines decreases as well, which inevitably requires a higher resolution for these lines in terms of line edge roughness (LER). The LER is related to the variation in thickness of the photoresist line along its length.[3] 25 nm photoresist lines with some LER are illustrated in Figure 1. From this scanning electron microscopy (SEM) picture, it can be clearly seen that the photoresist lines are not completely smooth along their lengths, which becomes even more problematic with the continuous feature size drop. It is therefore of utmost importance to be able to improve the LER of these mask lines, in order to fabricate next generation (and hence smaller) electronic features. One way to improve the LER is to pretreat the photoresist lines with a H_2 plasma.[4] In this process, the photoresist lines are mildly sputtered or etched in contact with a H_2 plasma, which results in a lower LER. A drawback of this pretreatment is that the original mask profile and size have been altered. Indeed, originally square-like mask lines can become so-called "mushroom-like" after H_2 plasma treatment.[4] This is exemplified in Figure 2. Figure 2a illustrates an original photoresist line. It has the desired square-like shape and size, but it suffers from undesired LER. After H_2 plasma treatment, the mask line has an improved LER, but the initial shape of the mask has been altered due to the pretreatment (Figure 2b). One way to restore the photoresist mask to its original profile and size, while keeping the improved LER, is to deposit a SiO_2 layer, also called a "capping layer" that selectively covers the photoresist line, as illustrated in Figure 2c. If the capping layer is properly created, trenches will be etched in the silicon surface in the next processing step, during which

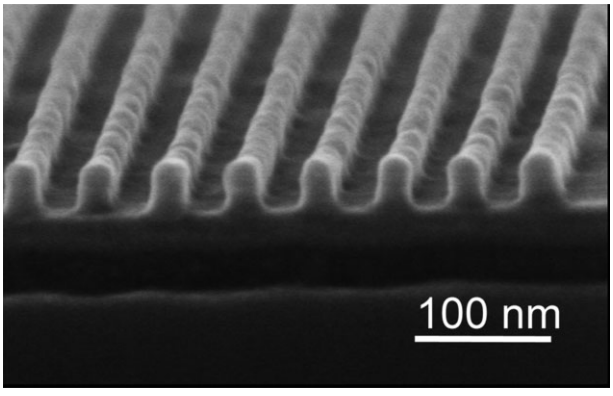


Figure 1. SEM picture of photoresist lines with line edge roughness for a pitch of 50 nm.

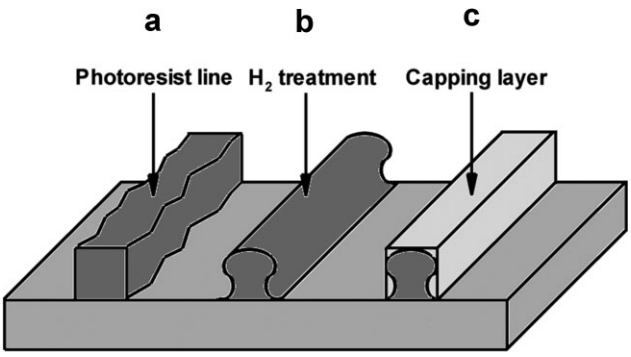


Figure 2. (a) The initial photoresist line with line edge roughness. (b) The photoresist line after treatment with H_2 plasma. The LER has improved but the original shape of the photoresist has been altered. (c) A SiO_2 film (i.e., the capping layer) covers the photoresist to restore the initial mask shape.

the capping layer, as well as part of the photoresist mask, are removed. Further removal of the residual photoresist after the etch process occurs with common removal techniques such as oxygen plasma treatments or wet removal with acetone and water rinsing. It is clear that creating this capping layer with the desired thickness on top of the mask, as well as on the sidewalls, while preventing the coverage on the Si wafer itself, is a challenging task and is, to the authors' knowledge, a process which is not yet optimized.

The goal of this paper is therefore to bring insight in how the formation of a SiO_2 capping layer can be controlled by tuning the plasma conditions in order to restore the photoresist profile to its desired original shape. For this purpose, a two-dimensional numerical model is used, which can simulate the deposition process of the capping layer on nanoscale mask lines for a range of different operating conditions. In this model, the plasma enhanced chemical vapor deposition (PECVD) process of SiO_2 with an $Ar/SiCl_4/O_2$ inductively coupled plasma (ICP) is considered. $SiCl_4/O_2$ is a proper gas mixture for depositing SiO_2-like films with good overall properties.[5–7] $SiCl_4$ dissociates in the plasma into non-volatile products ($SiCl_{0-3}$) which are the precursors for the deposition, while O_2 and O oxidize the deposited layer and convert it to SiO_2. Ar can be added to dilute the gas mixture, and control the overall deposition rate. Chlorine-containing gases are very effective for removing impurities, such as hydrogen (from the ambient air). Indeed, the only "by-product" in these mixtures is chlorine, which can remove the H impurities from the SiO_2 layer through the formation of HCl which diffuses out.[8] On the other hand, if the deposited SiO_2 film contains considerable amounts of residual chlorine, its mechanical stability decreases, and it becomes more susceptible to structural damage by ion sputtering from the plasma.[8] For the

application investigated in this paper, the SiO_2 film serves as a partial replacement of the photoresist, and thus should be as mechanically strong as possible to withstand high energy ion bombardment. It will therefore be key to avoid chlorine incorporation in the film, and to keep a high fraction of oxygen species in the gas mixture.

In the following sections, after a short description of the models, the shape and thickness of the capping layer will be discussed and explained based on the calculated fluxes of the species bombarding the wafer. Moreover, we will investigate the effect of gas pressure in the chamber, gas dilution with Ar, operating power, and substrate bias voltage on the overall shape of the capping layer, in order to find the optimum operating conditions.

2. Description of the Model

Two models are applied to investigate the SiO_2 capping layer formation. A plasma model, i.e., the so-called hybrid plasma equipment model (HPEM) developed by Kushner, is used to describe the bulk plasma behavior, and the fluxes of the plasma species toward the wafer. A more detailed explanation of this model can be found in this reference.[9] The reaction set that considers the $Ar/SiCl_4/O_2$ plasma chemistry has been presented and discussed in detail in another paper and thus will not be repeated here; however, a list of species included in the model is presented in Table 1.[10]

Furthermore, to predict the shape of the deposited SiO_2 capping layer on a mask line as a function of time, a nanoscale Monte Carlo (MC) simulation is performed.[11–14] This two-dimensional MC model uses the calculated fluxes, energy, and angular distributions from the HPEM as input to launch MC particles toward the nanoscale features. Also the created mesh, indicating the initial feature shape, and the material properties, are input parameters in this model, as well as the reaction set describing the surface processes. For the deposition process studied here, we have defined a total mesh with dimensions of 100 nm × 130 nm built up from 208 000 square computational cells with a surface area of 0.0625 nm^2. When a MC particle representing a depositing species (e.g., $SiCl_3$) arrives at a certain material cell (e.g., photoresist), a new cell is created on top consisting of $SiCl_{3(s)}$, based on the predefined reaction probability for deposition. Similarly, material cells can be removed by sputtering or etching reactions defined in the reaction set. This set, including the surface reaction probabilities, is also presented in detail in another paper,[10] and will only be briefly summarized here, i.e., the surface mechanism can be subdivided into four processes: (1) deposition of non-volatile products (i.e., $SiCl_3$, $SiCl_2$, SiCl, Si, SiO, and SiO_2), (2) oxidation of the surface (by O, O_2, and ClO), (3) chlorination of the surface, and (4) sputtering by ions. Furthermore, we consider the same surface reaction probabilities on all reactor walls since a coating (i.e., $\sim SiO_2$) will be deposited on all walls during plasma treatment. To define the oxidation of chlorinated silicon in the model, a step-wise oxidation is considered, where a chlorine atom is gradually replaced by an oxygen atom, eventually forming SiO_2. This mechanism has also been proposed by Cunge et al.[15] When a SiO_2 film is sputtered by ions from the plasma, the O atoms are sputtered preferentially, yielding a Si rich layer at the surface.[16–21] In addition, ions can also incorporate into the layer with the same probability as that of their neutral equivalents, which is the case for $SiCl_3^+$, $SiCl_2^+$, $SiCl^+$, Si^+, SiO^+ and SiO_2^+. Finally, if oxygen is sputtered preferentially and the layer becomes Si or $SiCl_x$ rich, chemical etching of the layer by chlorine can also occur.[22,23]

3. Results and Discussion

3.1. Model Validation

The reactor under study is the Lam Research 2300 Versys Kiyo 300 mm wafer ICP reactor.[24] This type of reactor has a planar coil on top of the reactor chamber, and is often referred to as a transformer coupled plasma (TCP) reactor with a centrally located gas nozzle in the top dielectric window.[10]

Calculations are performed for the following operating conditions: 13.56 MHz coil operating frequency, 10 mTorr

Table 1. Overview of the species included in the model. The species denoted with an (s) are surface layers.

Species	
Ground state neutrals:	Ar, Cl_2, Cl, O_2, O, ClO, Si, SiCl, $SiCl_2$, $SiCl_3$, $SiCl_4$, SiO, SiO_2
Positive ions:	Ar^+, Cl_2^+, Cl^+, O_2^+, O^+, ClO^+, Si^+, $SiCl^+$, $SiCl_2^+$, $SiCl_3^+$, $SiCl_4^+$, SiO^+, SiO_2^+
Excited species:	Ar^*, Cl^*, O^*
Negatively charged species:	Cl^-, O^-, electrons
Surface species:	$Si_{(s)}$, $SiCl_{(s)}$, $SiCl_{2(s)}$, $SiCl_{3(s)}$, $SiO_{(s)}$, $SiO_{2(s)}$, $SiClO_{(s)}$, $SiCl_2O_{(s)}$, $SiCl_3O_{(s)}$

Plasma Process. Polym. **2014,** *11*, 52–62

DOI: 10.1002/ppap.201300062

gas pressure, 300 W coil power, 60 °C wall, and substrate temperature, 120 °C dielectric window temperature, 5 sccm $SiCl_4$ and 20 sccm O_2 gas flow rate (hence without argon) and 15 s operating time. No bias voltage is applied for this purpose. The calculated shape of the deposited capping layer is shown in Figure 3a, and is compared with a transmission electron microscopy (TEM) picture of the capping layer obtained under the same operating conditions, as shown in Figure 3b, in order to validate the model. Because carrying out the deposition processes and taking successful TEM pictures can be laborious, performing simulations for different conditions is an interesting alternative for obtaining more insight in the deposition process in a shorter timescale. The calculated thickness of the capping layer is slightly overestimated, but in general there is a good agreement, both in shape and in absolute thickness, between the calculated and experimental profiles. Both show the highest deposition rate on top of the photoresist and the vertical deposition rate is higher than the horizontal one. Indeed, the capping layer is clearly thinner on the sidewalls than on top of the photoresist lines, which is not optimal. This anisotropic deposition process, where vertical deposition is dominant, can be explained by ion deposition. The calculated fluxes of the various species arriving at the center of the wafer are listed in Table 2. It is clear that the $SiCl_3$ and $SiCl_2$ radicals have the highest flux values besides the O atoms and O_2 molecules, so they account mainly for the $SiCl_x$ layer growth. The flux of SiCl is roughly 100 times lower than the flux values for $SiCl_2$ and $SiCl_3$, but it is still an important precursor due to its higher probability for deposition (i.e., 1.00 for SiCl vs. 0.05 for $SiCl_2$ and $SiCl_3$).[10] The fluxes of the other neutral depositing species (i.e., Si, SiO, and SiO_2) are even lower ($<10^{13}\,cm^{-2}\cdot s^{-1}$) and are not shown. Besides, the $SiCl^+_{1-3}$ ion fluxes are only about one order of magnitude lower than these neutral fluxes, so they will also contribute to $SiCl_x$ layer growth. Since no substrate bias is applied (see above), the ion energy at the wafer was calculated to be 10–12 eV, which is too low for significant sputtering, as the threshold for sputtering is typically around 20–30 eV for Si.[25] Therefore, the ions will be incorporated into the capping layer, accounting also for deposition. As most ions arrive perpendicular to the surface due to their acceleration through the sheath, this explains the higher vertical deposition rate. In addition, since a fraction of the ions and neutrals is lost at the sidewalls of the mask lines, the deposition rate at the bottom of the trenches between photoresist lines is slightly lower than on top of the mask lines.

Table 2. Calculated flux values (sorted by magnitude) of the relevant species involved in the growth of the SiO_2 capping layer.

Species	Flux [$cm^{-2}\cdot s^{-1}$]
O	2.22×10^{18}
O_2	3.12×10^{17}
$SiCl_3$	5.24×10^{15}
$SiCl_2$	1.56×10^{15}
$SiCl_3^+$	5.27×10^{14}
$SiCl^+$	6.00×10^{13}
$SiCl_2^+$	4.79×10^{13}
SiCl	2.90×10^{13}

The fact that the $SiCl^+_{1-3}$ ion fluxes toward the wafer are only about one order of magnitude lower than the $SiCl_3$ and $SiCl_2$ fluxes might be a bit unexpected, as their densities in the bulk plasma are about 100 times lower than the densities of their neutral equivalents. However, 95% of $SiCl_2$ and $SiCl_3$ is reflected from the surface, so there is not a strong density gradient near the walls and the net flux toward the wafer based on diffusion is relatively small.[10] This is not true for the ions, as they are accelerated through the sheath, and 100% lost at the walls (by wall neutralization). Moreover, $SiCl^+$ has an even higher flux to the wafer than SiCl. The volume averaged density of SiCl in the bulk plasma is about one order of magnitude higher than that of $SiCl^+$, but near the wafer surface, $SiCl^+$ obtains locally a higher density than SiCl, due to dissociative ionization of $SiCl_2$ into $SiCl^+$ and Cl. Indeed, the density of the parent molecule, $SiCl_2$, is typically maximum near the center of the wafer.[10] As it is clear from Table 2, the fluxes of O and O_2 are significantly higher than the $SiCl_x$ fluxes, due to the larger fraction of oxygen in the gas mixture (i.e, $O_2/SiCl_4$ ratio of 4; see above). This high $O_2/SiCl_4$ ratio is indeed necessary to ensure that

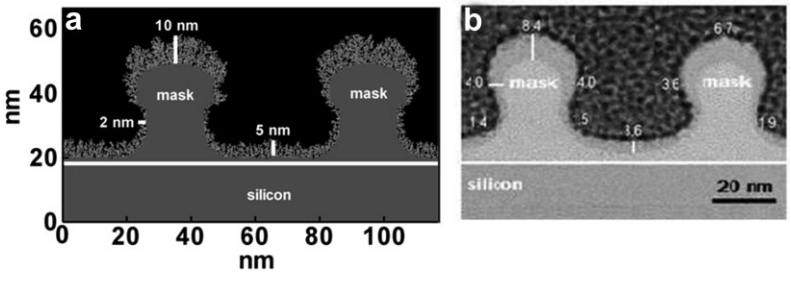


Figure 3. (a) Calculated and (b) measured values for a capping layer deposited at 13.56 MHz, 10 mTorr, 300 W, 60 °C wall and substrate temperature, 120 °C dielectric window temperature, 5 sccm $SiCl_4$, 20 sccm O_2, and 15 s operating time. The photoresist lines (or mask), the underlying silicon surface, as well as the thickness of the capping layer are indicated on both figures.

the deposited $SiCl_x$ layer is subsequently oxidized to near stoichiometric SiO_2 with minimal concentrations of trapped chlorine.[8]

In the next sections, we will explain how the capping layer profile can be altered by tuning the process parameters, including chamber pressure, dilution of the gas mixture with Ar, coil power, and applied bias to the substrate electrode.

3.2. Effect of Pressure

The calculated capping layer obtained at various pressures between 10 and 60 mTorr, keeping the other operating conditions constant, is presented in Figure 4. It is clear that the deposition process occurs faster at increased pressure. Indeed, at 60 mTorr, the deposited capping layer can reach a thickness of 30 nm after 15 s. This is due to a higher density, and hence higher flux to the wafer of the deposition precursors (i.e., mainly $SiCl_3$ and $SiCl_2$) at higher pressures (See Figure 5). Moreover, the deposition process is also more uniform at higher pressures, with a similar coating thickness on top of the photoresist lines and on the sidewalls. It should be noted that at 40 mTorr and higher, the capping layers on neighboring mask lines meet already after 15 s, creating a void between the lines and preventing further growth at the sidewalls. This eventually results in a non-uniform capping layer thickness, but initially (i.e., before a void is created), the deposition process was found to be very uniform at these pressures. The more isotropic deposition process at higher pressures is explained as it follows: an increase in gas pressure will entail a higher flux of $SiCl_3$ and $SiCl_2$ toward the wafer (see Figure 5), which are the main deposition precursors. Indeed, more $SiCl_4$ molecules are present in the plasma that will be dissociated by electron impact. The flux of SiCl, however, drops at higher pressure, because of an increased probability for recombination with Cl to form $SiCl_2$, due to the higher collision frequency at higher pressure.[10] O_2 is less easily dissociated into O atoms compared to $SiCl_4$ due to the strong double bond (5.16 eV). At constant operating power, it is therefore expected that the dissociation degree of O_2 decreases with increasing pressure; therefore, the O_2 flux rises whereas the O flux drops, leading to a higher flux of O_2 compared to O at a pressures above 15 mTorr. As far as the ion fluxes are concerned, near the top window of the reactor, underneath the coil (i.e., where power deposition is highest), more ions will be created due to a higher gas density at higher pressure; simultaneously, more ions will be lost in neutralization reactions when migrating from the high plasma density region (near the top window) toward the wafer. This eventually results in a drop of ion fluxes toward the wafer at higher pressures, as it is apparent

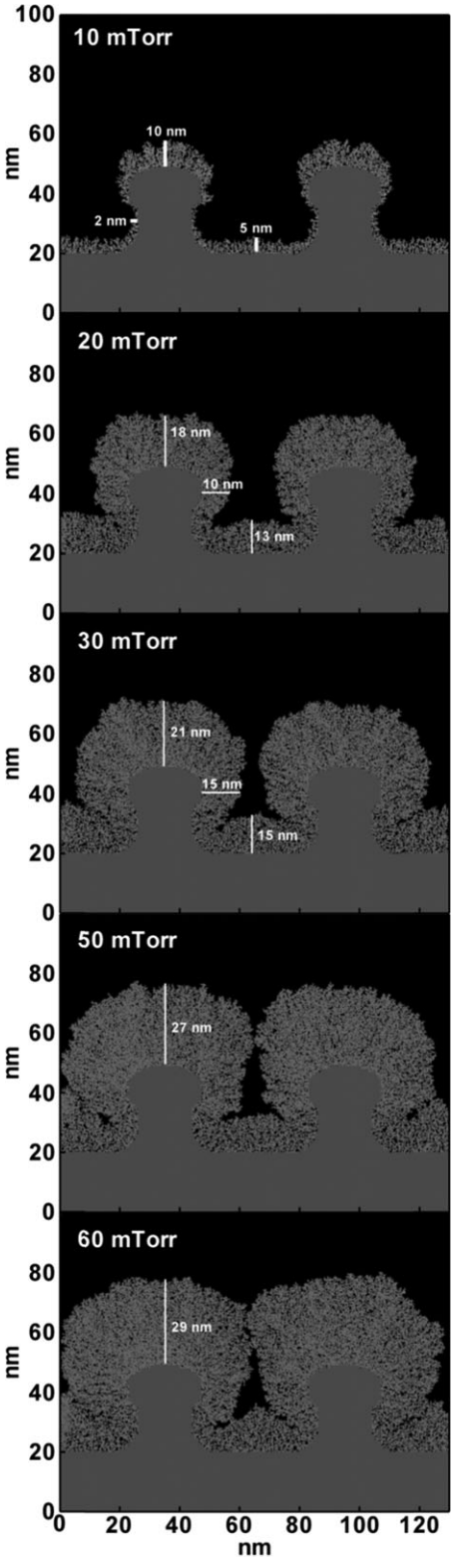


Figure 4. Calculated capping layer profiles for 10–60 mTorr gas pressure in plasma chamber. The other operating conditions are the same as those presented in Figure 3.

Plasma Process. Polym. **2014,** *11*, 52–62

DOI: 10.1002/ppap.201300062

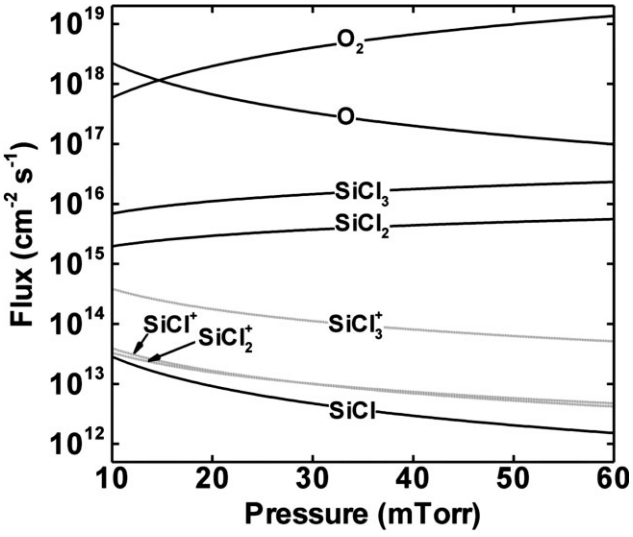


Figure 5. Calculated values for the flux toward the center of the wafer of the relevant species involved in the capping layer deposition as a function of pressure. The ion fluxes are plotted in gray for clarity. The other operating conditions are the same as those listed in Figure 3.

from Figure 5. The latter will affect the shape of the capping layer. Indeed, the vertical deposition is now not favored anymore, and a more isotropic deposition process will occur, as it could be deduced from Figure 4.

Also, at higher pressures the ion angular distribution is wider, as is illustrated in Figure 6, which further enhances the isotropy of the deposition process. This

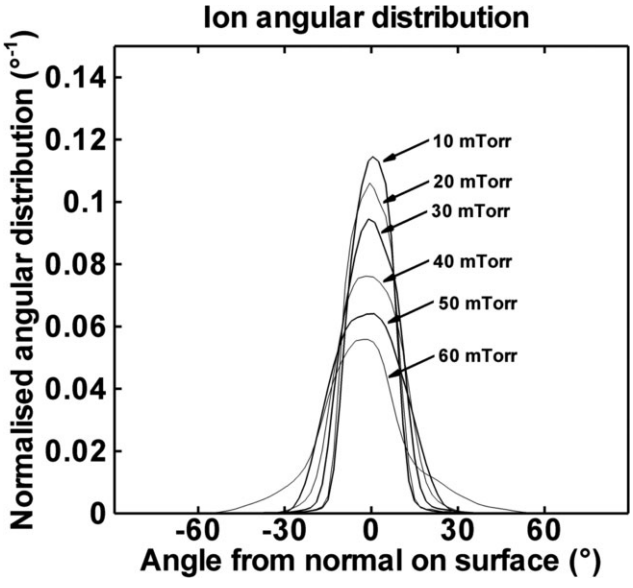


Figure 6. Calculated ion angular distributions for 10–60 mTorr gas pressure. The other operating conditions are the same as those listed in Figure 3.

effect, however, is less significant compared to the increased ratio of neutral flux over ion flux.

We can conclude that a higher pressure will give rise to a more isotropic, and hence more uniform deposition process as it is desired; however the disadvantage is that the bottom of the trench is also covered at the same rate, which should be avoided. Indeed, only the mask lines should be covered with a capping SiO_2 layer. Furthermore, at higher pressure, the deposition rate quickly becomes too high. For growing a capping layer of only a few nm thick, the operating time must therefore be in the order of a few seconds. This can create problems in terms of wafer-after-wafer repeatability, because, at the start of the deposition process, plasma typically needs 2–5 s to stabilize. In the case of a very short operating time, this stabilization time takes up a large fraction of the total processing time, increasing the chance for fluctuations in successive processes.

3.3. Effect of Ar Dilution

As mentioned in the Section 3.2 above, a higher pressure has the advantage of an improved capping layer thickness uniformity on both the vertical and horizontal surfaces. Moreover, it yields an increased uniformity across the wafer, as is discussed in another paper.[10] Unfortunately, as also mentioned above, a too high deposition rate is also found, creating a film which is already too thick after a few seconds. To overcome this problem, the gas mixture can be diluted by adding a non-reactive gas, such as Ar. This way, the overall deposition rate can be controlled while working at higher operating pressure. This can be useful if only a very thin film is required, as is the case for the capping layer (see discussion in Section 3.2 above). The calculated fluxes of the relevant species bombarding the wafer, at the same conditions as in Figure 3, are plotted in Figure 7 as a function of Ar dilution. The flux of Ar^+ ions is also included. Ar atoms are chemically inert, and will not account for deposition or chemical reactions at the wafer surface, and are therefore not important in this context, but Ar^+ ions can account for physical sputtering of the surface, at least when a bias voltage would be applied. As expected, the fluxes of the oxidizing species (i.e., O and O_2) and of the depositing species (i.e., $SiCl_3$, $SiCl_2$, and SiCl) drop linearly with increasing the Ar concentration, but the relative ratios remain the same. The $SiCl_{1-3}^+$ ion fluxes also decrease when diluting with Ar, but the drop is somewhat less pronounced. The reason is that charge transfer reactions of Ar^+ with $SiCl_{1-3}$ neutrals are an important source for the formation of the $SiCl_{1-3}^+$ ions, so their densities and fluxes do not decrease as much as the neutrals upon dilution with Ar. For the same reason, it is interesting to mention that Ar^+ ions become dominant only above 80% Ar fraction in the gas mixture.

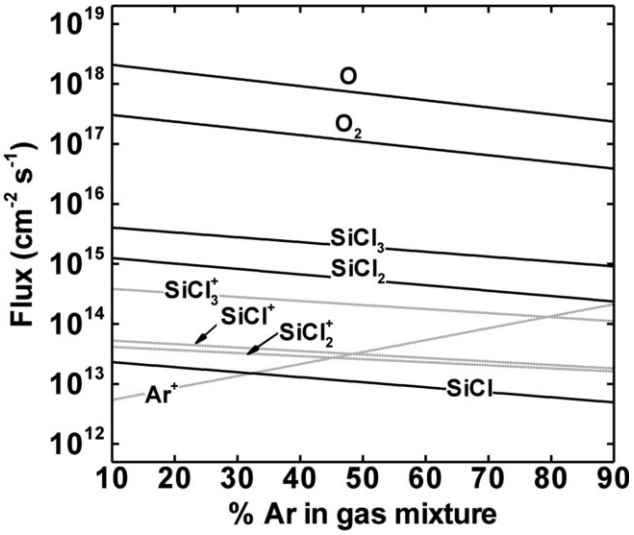


Figure 7. Calculated values for the flux toward the center of the wafer of the relevant species involved in the capping layer formation, as a function of Ar dilution. The other operating conditions are the same as as those listed in Figure 3.

Figure 8 shows the calculated capping layer profiles for different dilutions with Ar. The film thickness clearly decreases with increasing the Ar concentration due to the lower fluxes of the depositing precursors. However, the thickness uniformity of the capping layer does not really improve. Indeed, as is seen in Figure 7, the drop in ion fluxes that account for the deposition is less pronounced than for the neutral fluxes. Thus, at higher Ar concentrations, the ratio of ion fluxes over neutral fluxes is larger, and consequently the contribution of vertical deposition is slightly more pronounced. This explains why the deposition process becomes slightly more anisotropic compared to the non-diluted case, with somewhat more pronounced vertical deposition versus sidewall deposition, although this is not clearly visible from the figure, as the deposited film is very thin under strong dilutions.

3.4. Effect of Power

The calculated shapes of the capping layers obtained at different operating powers ranging from 200 to 1 200 W, while keeping the other conditions constant, are shown in Figure 9. The shape of the capping layer becomes more anisotropic with increasing the applied power. For instance, at 400 W, the ratio of vertical deposition over lateral deposition is about 1.8, whereas it is 6.25 at 1 200 W. As mentioned earlier, vertical deposition is mainly due to non-volatile ions ($SiCl_{1-3}^+$), and as it can be seen in Figure 10, these ion fluxes toward the wafer indeed rise with increasing the power. The fluxes of

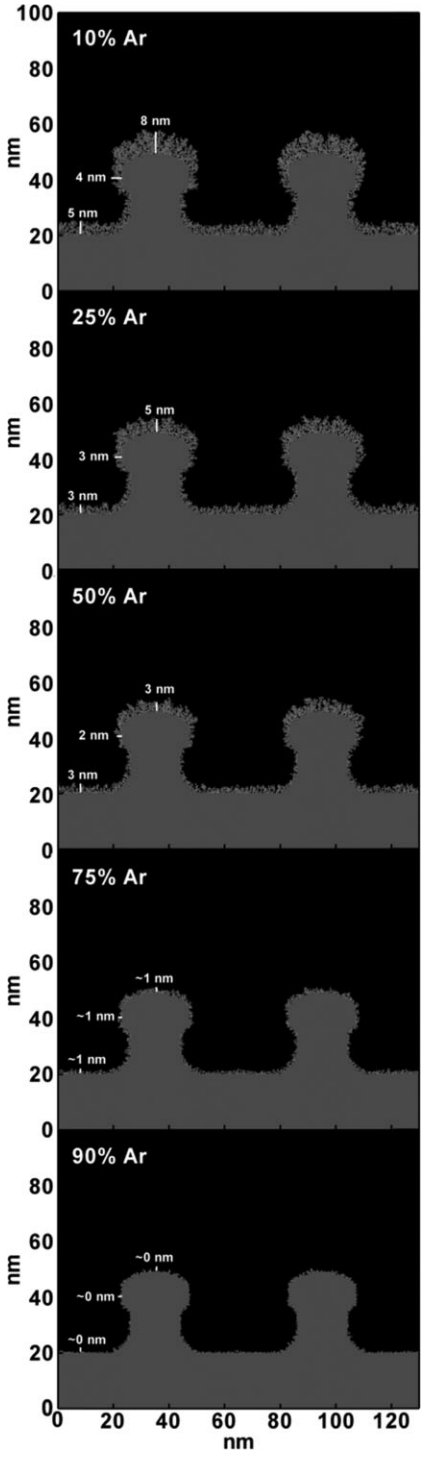


Figure 8. Calculated capping layer profiles obtained at gas mixtures diluted with 10–90% Ar. The other operating conditions are the same as those listed in Figure 3.

the neutral precursors (i.e., $SiCl_{1-3}$) increase with increasing the power as well, which explains the overall higher deposition rate; however, the measure of anisotropy is dependent on the ratio of the $SiCl_{1-3}^+$ ion fluxes over the

Plasma Process. Polym. **2014,** *11*, 52–62

DOI: 10.1002/ppap.201300062

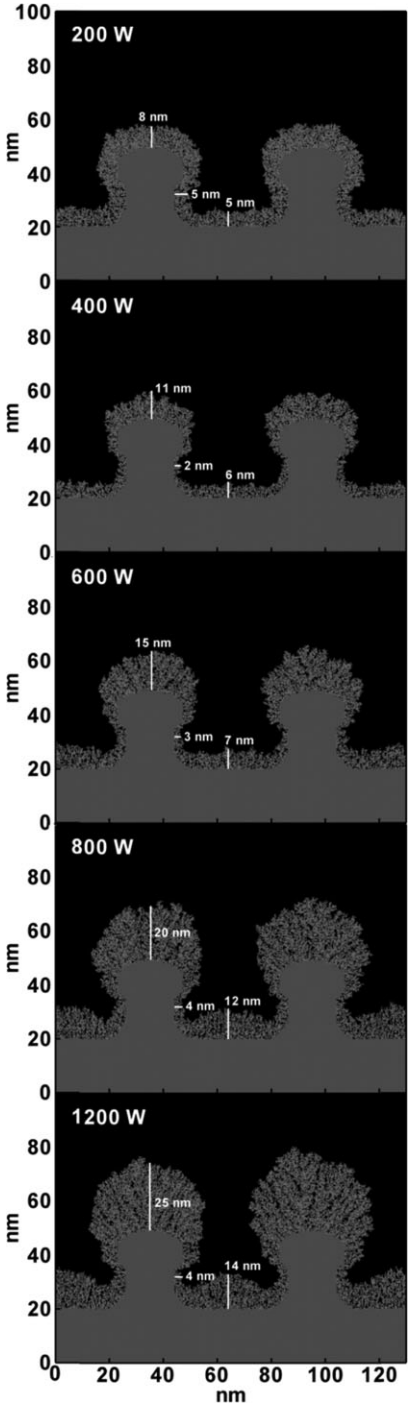


Figure 9. Calculated capping layer profiles at 200–1 200 W coil power. The other operating conditions are the same as those listed in Figure 3.

$SiCl_{1-3}$ neutral fluxes, which is indeed larger at higher power (see Figure 10). This is expected because the free electrons will be more strongly accelerated at higher powers, and more ionization and dissociation reactions will occur, yielding higher ion and precursor

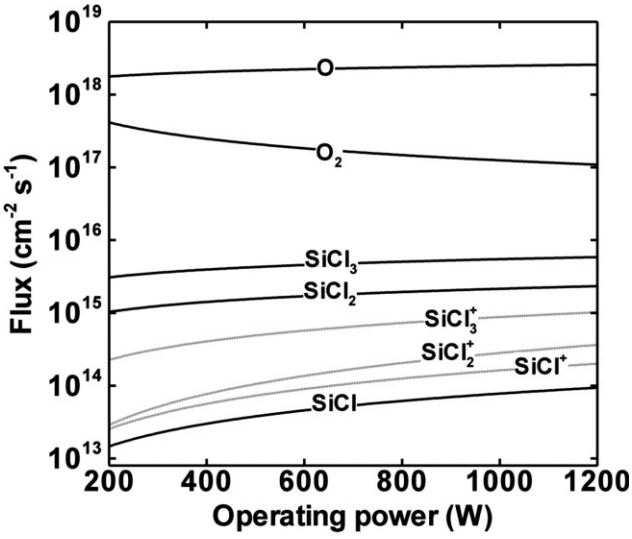


Figure 10. Calculated values for the flux toward the center of the wafer of the relevant species involved in the capping layer deposition, as a function of operating power. The other operating conditions are the same as those listed in Figure 3.

fluxes towards the wafer. For the same reason, the O_2 flux drops with increasing the power, and the O flux increases slightly, because the dissociation of O_2 becomes also more important at higher powers. It can be concluded that an increase in power does not seem to be beneficial for the capping layer growth. The overall deposition rate, as well as the anisotropy rises with increasing the power, so the best conditions for capping layer formation should be at mild operating powers (see result at 200 W in Figure 9).

3.5. Effect of the Bias Voltage

We have also performed calculations when applying a bias on the substrate electrode, keeping the other conditions constant. The calculated capping layer profiles obtained for a bias voltage ranging from −50 to −250 V are presented in Figure 11. Adding a substrate bias to the original recipe seems to have very promising effects on the capping layer growth. As it is clear from this figure, as the bias voltage becomes stronger, the vertical deposition rate is reduced, and, at the same time, sidewall deposition seems to be enhanced, as desired.

It is well known that a substrate bias controls the energy of the ions when bombarding the wafer, while the magnitudes of the fluxes are mainly dependent on the applied coil power and to a lower extent on the bias voltage. Indeed, for the conditions with bias, the fluxes of all relevant species were found to be very similar to those shown in Table 2, where no bias was applied. Without bias, the average ion energy is about 12 eV, which is too low for

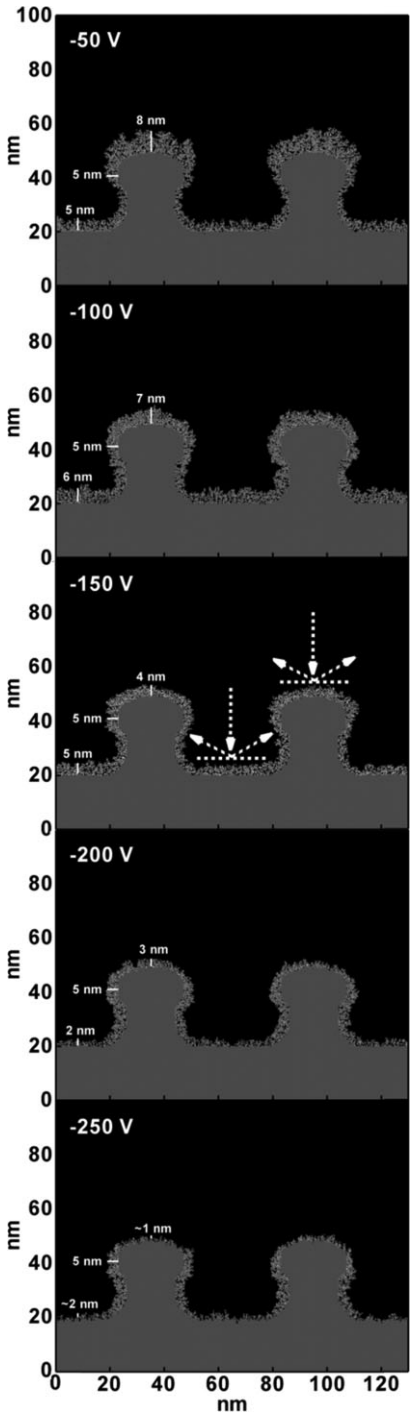


Figure 11. Calculated capping layer profiles for substrate bias voltages of −50 to −250 V. The other operating conditions are the same as those listed in Figure 3. The white dashed arrows at −150 V illustrate how the ions sputter the horizontal surfaces and how products subsequently can redeposit on the sidewalls.

sputtering, but the ion energies obtained in the cases with bias voltage are much higher than the threshold for sputtering (20–30 eV), as it is clear from Figure 12. The ion energy distributions at non-zero bias voltages typically

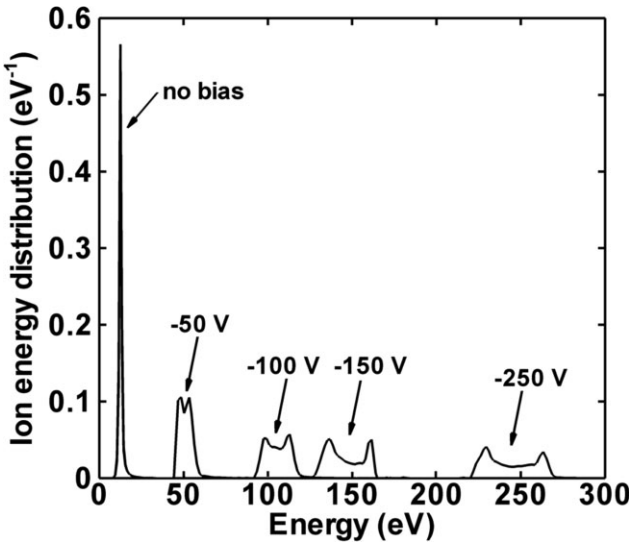


Figure 12. Calculated energy distributions of the ions arriving at the center of the wafer for different bias voltages, ranging from no bias to −250 V. The other operating conditions are the same as those listed in Figure 3.

have two maxima due to the radiofrequent (rf) voltage applied on the substrate electrode for creating the desired dc bias. The two maxima in the distributions correspond to the maximum and minimum voltages within the rf cycle. Thus, besides ion deposition, also a considerable amount of sputtering of the layer will occur in these cases. This way, by tuning the bias voltage, one can control the ratio between ion deposition and ion sputtering, hence controlling the vertical deposition rate. Besides the fact that the capping layer is thinner on top of the mask and at the bottom of the trench between mask lines due to sputtering, the layer deposited on the sidewalls is slightly thicker as well, compared to the case without bias. This is due to redeposition of sputtered species from the trench bottom onto the sidewalls, as illustrated by the dashed white arrows in the profile at −150 V in Figure 11.

It can therefore be concluded that the ratio between vertical and lateral deposition can be strongly influenced by the energy of the ions arriving at the wafer, which can be steered by the substrate bias. In fact, this ratio is not only influenced by the energy of the ions, but also by their angular distribution. At stronger bias voltage, the ions tend to bombard the surface more vertically, as is illustrated in Figure 13, which further enlarges the ratio between vertical and lateral deposition. Finally, it should be mentioned that a high bias voltage will not result in significant damage of the mask or the underlying silicon if the capping layer is created properly. Indeed, under the right conditions, the SiO_2 layer is still grown, but sputtered at the same time to limit its thickness and to control its shape.

Plasma Process. Polym. **2014,** *11*, 52–62

DOI: 10.1002/ppap.201300062

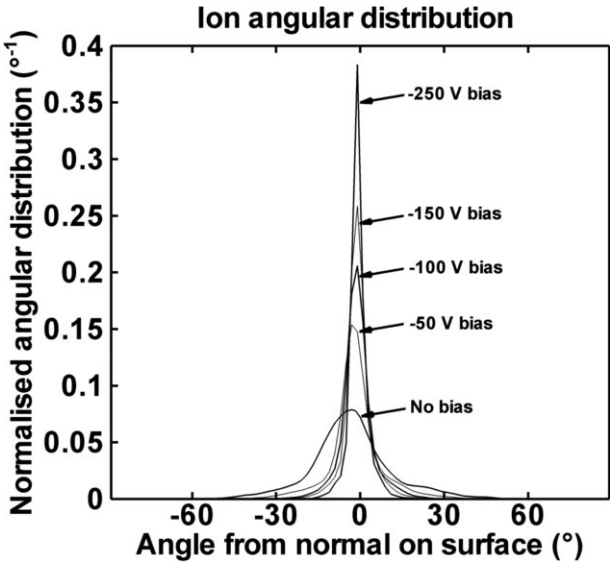


Figure 13. Calculated ion angular distributions at bias voltages ranging from 0 to −250 V. The other operating conditions are the same as those listed in Figure 3.

4. Conclusions

The deposition process of a SiO_2 capping layer with an $Ar/SiCl_4/O_2$ ICP has been investigated numerically in order to obtain more insight in the capping layer formation process. This layer is deposited over the photoresist mask lines, in order to restore their original shape. The calculated two-dimensional shape of the capping layer is presented and explained based on the fluxes of the plasma species bombarding the wafer. The most important precursors for deposition are $SiCl_3$, $SiCl_2$ and SiCl neutrals, as well as $SiCl_3^+$, $SiCl_2^+$ and $SiCl^+$ ions. Sputtering of the layer by ions was found to be negligible when no bias is applied. The most important species for oxidation of the deposited $SiCl_x$ film, to form a SiO_2 capping layer, are O and O_2. In this work, we have mainly focused on the shape of the capping layer and not on the film composition. However, it could be concluded that under all investigated operating conditions the film was near stoichiometric SiO_2 with very small amounts of residual chlorine (i.e., less than 1%), which is indeed required for a good mechanical stability. It was found that the capping layer was thicker on top of the photoresist and at the bottom between photoresist lines, compared to the sidewalls, under the operating conditions typically used in experiments, suggesting a dominant vertical deposition rate due to the important contribution of the vertically arriving ions. This calculated capping layer shape was validated by comparing with TEM measurements. Furthermore, the effects of chamber pressure, gas dilution with Ar, operating power and bias voltage were investigated, to find out how to improve the capping layer shape. Increasing the gas pressure results in a higher ratio of neutral flux over ion flux, creating a more isotropic deposition process. However, it also results in a too high deposition rate, yielding a capping layer which is too thick. This is less practical in terms of process stability and repeatability, as the plasma needs some time to stabilize after ignition.

Diluting the $SiCl_4/O_2$ mixture with Ar results in a decrease of the overall deposition rate, which allows a longer operating times, and therefore more control of the wafer-after-wafer reproducibility, especially if the processing time is only a few seconds. However, it does not simply result in an identical capping layer shape with a thickness linearly correlated to the dilution. This is due to significant charge transfer of Ar^+ ions with $SiCl_3$ and $SiCl_2$ to form $SiCl_3^+$ and $SiCl_2^+$ ions that account for vertical deposition, resulting in a somewhat different shape of the capping layer as a function of gas dilution. A higher operating power results in a lower ratio of neutrals over ions, creating a more anisotropic deposition process. For an optimal capping layer shape, mild operating powers seem to be more appropriate. Finally, applying a bias voltage has no significant effect on the magnitude of the fluxes of the relevant species, but greatly influences the energy of the ions bombarding the wafer, allowing control over the vertical deposition rate due to sputtering. In addition, the sidewall deposition is increased due to redeposition of sputtered products. The bias voltage therefore has a strong influence on the resulting capping layer profile, and seems to be a useful process parameter for optimizing the capping layer growth. Generally, this research has shown that the shape of the SiO_2 capping layer is significantly dependent on the chosen operating conditions. Therefore, process parameters must be chosen carefully to ensure a good balance between sidewall and vertical deposition. Although the bias voltage allows for most control of the thickness and the shape of the capping layer, a desired SiO_2 film can only be created if all other operating conditions are chosen properly as well, to ensure the correct but delicate balance between deposition and sputtering.

Acknowledgements: The Research Foundation Flanders (FWO) is acknowledged for financial support of this work. The authors thank M. Kushner for providing the code and useful advice. This work was carried out in part using the Turing HPC infrastructure at the CalcUA core facility of the Universiteit Antwerpen, a division of the Flemish Supercomputer Center VSC, funded by the Hercules Foundation, the Flemish Government (department EWI) and the University of Antwerp.

Received: May 21, 2013; Revised: September 6, 2013; Accepted: September 26, 2013; DOI: 10.1002/ppap.201300062

Keywords: deposition process; inductively coupled plasmas (ICP); modeling; plasma-enhanced chemical vapor deposition (PECVD); SiO_2 nano-layers

[1] G. Moore, *Electronics* **1965**, *38*, 8.
[2] International Technology Roadmap for Semiconductors homepage, www.itrs.net, August 2013.
[3] E. Gogolides, V. Constantoudis, G. P. Patsis, A. Tserepi, *Microelectron. Eng.* **2006**, *83*, 1067.
[4] E. Altamirano-Sánchez, A. V. Pret, R. Gronheid, W. Boullart, *Proc. SPIE – Int. Soc. Opt Eng.* **2012**, *8328*, 832802.
[5] J. C. Alonso, R. Vasquez, A. Ortiz, V. Pankov, E. Andrade, *J. Vac. Sci. Technol. A* **1998**, *16*, 3211.
[6] A. Ortiz, C. Falcony, M. Farias, L. Cota-Araiza, G. Soto, *Thin Solid Films* **1991**, *206*, 6.
[7] J. C. Alonso, E. Pichardo, L. Rodriguez-Fernandes, J. C. Cheang-Wong, A. Ortiz, *J. Vac. Sci. Technol. A* **2001**, *19*, 507.
[8] A. Ortiz, S. Lopez, C. Falcony, M. Farias, L. Cota-Araiza, G. Soto, *J. Electron. Mater.* **1990**, *19*, 1411.
[9] M. J. Kushner, *J. Phys. D: Appl. Phys.* **2009**, *42*, 194013.
[10] S. Tinck, A. Bogaerts, *Plasma Process. Polym.* **2013**, *10*, 714.
[11] D. Zhang, *PhD Thesis*, University of Illinois (Urbana, Illinois, USA) **2000**.
[12] R. Hoekstra, *PhD Thesis*, University of Illinois (Urbana, Illinois, USA) **1998**.
[13] V. Vyas, *PhD thesis*, University of Illinois (Urbana, Illinois, USA) **2005**.
[14] A. Sankaran, *PhD Thesis*, University of Illinois (Urbana, Illinois, USA) **2003**.
[15] G. Cunge, D. Vempaire, R. Ramos, M. Touzeau, O. Joubert, P. Bodard, N. Sadeghi, *Plasma Sources Sci. Technol.* **2010**, *19*, 034017.
[16] D. H. Kim, G. H. Lee, S. Y. Lee, D. H. Kim, *J. Cryst. Growth* **2006**, *286*, 71.
[17] E. Collart, R. J. Visser, *Surf. Sci. Lett.* **1989**, *218*, L497.
[18] B. Lang, *Appl. Surf. Sci.* **1989**, *37*, 63.
[19] V. S. Smentkowski, *Prog. Surf. Sci.* **2000**, *64*, 1.
[20] T. Mizutani, *J. Non-Cryst. Sol.* **1995**, *181*, 123.
[21] M. P. Seah, T. S. Nunney, *J. Phys. D: Appl. Phys.* **2010**, *43*, 253001.
[22] G. Cunge, N. Sadeghi, R. Ramos, *J. Appl. Phys.* **2007**, *102*, 093305.
[23] R. J. Hoekstra, M. J. Grapperhaus, M. J. Kushner, *J. Vac. Sci. Technol. A* **1997**, *15*, 1913.
[24] Lam Research Corporation, www.lamrc.com, August 2013.
[25] N. Matsunami, Y. Yamamura, Y. Itikawa, N. Itoh, Y. Kazumata, S. Miyagawa, K. Morita, R. Shimizu, H. Tawara, *At. Data Nuc. Data Tables* **1984**, *31*, 1.

DOI: 10.1002/ppap.201300062